ABSTRACT OF THE INVENTION

Disclosed is a method of testing memory, comprising providing one or more semiconductor wafers having one or more semiconductor chips thereon, each said chip comprising one or more memory cells, providing a programmable testing apparatus comprising at least one test pattern generators and a test bed adapted to receive said one or more wafers in communicative contact so as to address individual memory cells, chips, and wafers and transmit information thereto and receive information therefrom, receiving one or more test commands, constructing a test sequence of one or more commanded tests from said test commands, constructing at least one header comprising location information for each said wafer, chip and memory cell, testing said memory cells with a test pattern generated by said test pattern generator, collecting the results of said testing and passing them to a display device, passing said location information to said display device, constructing and displaying a graphical representation of said test results using said location information.